

Customer No.: 31561  
Application No.: 10/604,169  
Docket No.: 10969-US-PA

AMENDMENTS

To the Claims:

Please amend the claims as follows:

1. (currently amended) A band pass filter (BPF) for extracting a desired frequency band from an input signal that is represented in a sequence of data stream, comprising:

a shift register for receiving the input signal and synchronously moving the input signal data stream through the shift register so that the input signal goes into an input end and comes out from an output end of the shift register, wherein between the input and output ends of the shift register, a segment of the input data is stored, and as the input signal and time go by, the input signal segment stored in the shift register is sliding through a whole input signal spectrum; and

an arithmetic subtracting unit for obtaining a difference between only an input data stored in the output end of the shift register and an input data stored in the input end of the shift register to form an output of the band pass filter.

2. (original) The band pass filter of claim 1, wherein the shift register comprises a plurality of registers that are coupled in cascade to form a serial-in shift register that has a data input end and a data output end, and receives an input signal from the data input end register.

3. (original) The band pass filter of claim 1, wherein the means for synchronously moving the input signal data stream through the shift register is a synchronization clock.

Customer No.: 31561  
Application No.: 10/604,169  
Docket No.: 10969-US-PA

4. (original) The band pass filter of claim 1, wherein the arithmetic subtracting unit subtracts an input data stored in the output end of the shift register from an input data stored in the input end of the shift register to form an output of the band pass filter.

5. (original) The band pass filter of claim 1, wherein the length of the input signal segment stored in the shift register is determined by a sum of one and an integer part of a ratio of a half of a signal sampling rate of the input signal to a desired band pass frequency.

6. (original) The band pass filter of claim 1, wherein each of the registers has a storage capacity of at least one bit of digital data.

7. (original) The band pass filter of claim 1, wherein each of the registers can store a numeric value.

8. (original) The band pass filter of claim 1, wherein the arithmetic subtracting unit comprises an adder and an inverter that is coupled to an input end of the adder.

9. (currently amended) A method of obtaining a desired frequency band from an input signal for a band pass filter, which comprises:

receiving the input signal based on a time frame;

marking currently received data as a present reference;

recording a segment of the input signal from the present reference on as the input signal and time go by; and

sequentially reporting a difference between the ends of the recorded input signal segment to obtain an output of the method based on the time frame[. . .];

providing a number of registers coupled in cascade to form a shift register.

Customer No.: 31561  
Application No.: 10/604,169  
Docket No.: 10969-US-PA

having a first register and a last register, wherein each register has a storage capacity of at least one bit; and

computing a difference of contents stored only in the first register and the last register to form an output of the method in a clock frame.

10. (original) The method of claim 9, a length of the memorized input data segment is determined by a ratio of a half of a sampling rate of the input signal to a target desired frequency of the method.

11. (original) The method of claim 9, during a boundary condition, a beginning of the method or an ending of the method, zeros are inserted to both ends of the input data sequence.

12. (currently amended) A method of obtaining a desired frequency band from an input signal for a band pass filter, comprising:

providing a number of registers coupled in cascade to form a shift register, having a first register and a last register, wherein each register has a storage capacity of at least one bit; and

computing a difference of contents stored only in the first register and the last register to form an output of the method in a clock frame.

13. (original) The method of claim 12, wherein the number of registers is determined by adding one to an integer part of a ratio of a half of the input signal sampling rate to a target desired frequency of the method.

14. (original) The method of claim 12, wherein the difference of contents stored in the first and last registers is calculated by adding a content of the first register

Customer No.: 31561  
Application No.: 10/604,169  
Docket No.: 10969-US-PA

and a negative content of the last register to form an output of the method in the clock frame.

15. (original) The method of claim 12, wherein a register in the shift register stores digital data.

16. (original) The method of claim 12, wherein a register in the shift register stores numeric data.

17. (original) The method of claim 9, wherein the method receives the input signal under a synchronization clock.